Amendments to the Specification:

Please replace paragraph **[0003]** with the following amended paragraph:

[0003] A third approach is to monolithically integrate the Schottky diode and the power MOSFET. This monolithic solution avoids issues with connection parasitics and allows considerably more flexibility in implementing the Schottky structure. Korman et al., for example, disclose in U. S. Pat. No. 5,111,253 a planar vertical double diffused MOSFET (DMOS) device with a Schottky barrier structure. A similar structure is described by Cogan in U.S. Pat. No. 4,811,065 where again a Schottky diode is monolithically integrated on the same silicon substrate as a lateral DMOS device. These devices, however, have been limited to planar power MOSFET technology. The monolithic Schottky diode structures used in these types of devices do not lend themselves well to power MOSFET devices using trench technology. A monolithic trenched gate MOSFET and MOS enhanced Schottky diode structure is disclosed by S. P. Sapp in the commonly assigned U. S. Patent No. ~~5,111,253~~ 6,351,018 incorporated herein by reference. Although this integrated trench power MOSFET has improved the overall performance of the trench MOSFET for particular applications, the full potential of this technology has not yet been realized.

Please replace paragraph **[0029]** with the following amended paragraph:

[0029] The present invention is not limited to the particular trench structure shown in FIG. 1. For example, in an alternate embodiment shown in FIG. 3, the polysilicon layers filling the trenches are recessed and covered by a dielectric layer (e.g., oxide) 300. Thus, when the Schottky anode/ MOSFET source metal layer 302 is deposited, the polysilicon layers in the trenches of the Schottky structure remain isolated. The polysilicon layers in the trenches of the Schottky structure can thus float or connect to the gate poly inside the MOSFET trenches. In other embodiments, each trench structure includes electrodes buried under a gate electrode as shown in FIGs. 4A and 4B. In FIG. 4A, MOSFET 400B includes active trenches 402B each having electrodes 411 buried under a gate electrode 410. A Schottky diode 428B is formed

between two trenches 402L and 402R as shown. The charge balancing effect of biased electrodes 411 allows for increasing the doping concentration of the drift region without compromising the reverse blocking voltage. Higher doping concentration in the drift region in turn reduces the forward voltage drop for this structure. The depth of each trench as well as the number of the buried electrodes may vary. In the FIG. ~~4C~~ 4B variation, trench 402C has only one buried electrode 411, and gate electrodes 410S in the trenches flanking Schottky diode 428C connect to the source electrode as shown. Gate electrodes 410S can alternatively connect to the gate terminal of the MOSFET. In yet another embodiment, the oxide thickness along the bottom of the trenches is made thicker than that along the trench sidewalls to advantageously reduce the gate to drain capacitance.

Please replace paragraph **[0031]** with the following amended paragraph:

[0031] The silicon data was obtained ~~form~~ from an integrated Schottky structure built on a 0.35m trench DMOS baseline process flow. The trench depth is 1m and the gate oxide is 400Å. The starting material is 0.25 Ohm-cm and the Schottky interface used is Titanium with a work function of 4.3eV. These values are merely illustrative and not intended to be limiting. The simulation data was obtained using device simulator Medici. The mixed-mode circuit-device capability of Medici, combining finite element device models with nodal analysis of SPICE, is well suited for the intended device and circuit simulations. The simulation circuit for the diode recovery along with an example waveform for modeling diode recovery are shown in FIG. 5. The MOSFET-Schottky structure used in the modeling is shown FIG. 6.

Please replace paragraph **[0036]** with the following amended paragraph:

[0036] FIG. 14 shows a detailed view of the MOSFET-Schottky structure sub-circuit shown in FIG. 5. Various current components are identified in FIG. 14. FIG. 15 shows the normalized gate displacement current during the device recovery for the cases of the 2.5% and 50% Schottky structure contribution. As ~~show~~ shown, the maximum current contribution of the gate terminal represents approximately half of the maximum total recovery current for the 2.5% Schottky

structure contribution. In the case of 50% contribution, the gate current makes up about 20% of the maximum current. This current is due to the gate-drain capacitance in the MOSFET and is thus a displacement current which is injected into the total recovery value as a consequence of the testing circuit configuration shown in FIG. 5.